AFTER FINAL EXPEDITED PROCEDURE

This listing of claims replaces all prior versions, and listings of claims in the instant application:

Listing of Claims:

1. (Previously Presented) A processor comprising:

a bus for carrying at least a portion of an instruction instance identifier;

a branch prediction storage, connected to said bus, including:

branch direction storage, connected to said bus and having a first output for providing a branch direction indication, for storing entries for branch direction indications,

wherein each branch direction indication stored in said branch direction storage indicates a direction of a branch instruction instance with respect to branch prediction; and

in response to said at least a portion of said instruction instance identifier, a branch direction indication associated with that instruction instance identifier is provided on said first output; and

branch prediction qualifier indications storage connected to at least a portion of said bus and having a second output for providing a branch predication qualifier indication, for storing entries for branch prediction qualifier indications,

wherein in response a signal on said at least a portion of said bus, a branch prediction qualifier indication associated with said at least a portion of said instruction instance identifier is provided on said second output;

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wherein said entries in said branch direction indications storage are more numerous than said entries in said branch prediction qualifier indications storage; and

an outcome of said branch instruction instance is predicted based at least in part on said branch direction indication on said first output and said branch prediction qualifier indication on said second output.

2. (Previously Presented) The processor of claim 1 wherein, during execution of program code on the processor, at least some of the branch prediction qualifier entries are associated with multiple ones of the branch direction entries.

3. (Original) The processor of claim 1 wherein the branch direction indications and the branch prediction qualifier indications are accessible based at least in part on one or more of instruction instance identifiers and gshare addresses.

4. (Previously Presented) The processor of claim 3 wherein the branch prediction qualifier indications are accessible based at least in part on one or more of least significant bits of the instruction instance identifiers and least significant bits of the gshare addresses.

5. (Previously Presented) The processor of claim 3 wherein the instruction instance identifiers comprise one of program counters, physical addresses, and virtual addresses.

6. (Previously Presented) The processor of claim 1 wherein the branch prediction storage comprises storage for one or more of branch history pattern indications and branch target instruction instance identifiers.

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7. (Previously Presented) The processor of claim 1 wherein the branch direction indications comprise one or more bits that indicate one or more of branch history, branch prediction, and branch pattern.

8. (Previously Presented) The processor of claim 1 wherein the branch prediction qualifier indications comprise one or more bits that indicate one or more of confidence, strength, and validity of branch direction indications.

9. (Previously Presented) A branch prediction storage structure including:

branch direction storage, connected to a bus for carrying at least a portion of an instruction instance identifier and having a first output for providing a branch direction indication, for storing entries for branch direction indications,

wherein each branch direction indication stored in said branch direction storage indicates a direction of a branch instruction instance with respect to branch prediction; and

in response to said at least a portion of said instruction instance identifier, a branch direction indication associated with that instruction instance identifier is provided on said first output; and

branch prediction qualifier indications storage, connected to at least a portion of said bus and having a second output for providing a branch predication qualifier indication, for storing entries for branch prediction qualifier indications

wherein in response a signal on said at least a portion of said bus, a branch prediction

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qualifier indication associated with said at least a portion of said instruction instance identifier is provided on said second output;

the branch direction indication entries are more numerous than the branch prediction qualifier indications; and

an outcome of said branch instruction instance is predicted based at least in part on said branch direction indication on said first output and said branch prediction qualifier indication on said second output.

10. (Original) The branch prediction storage of claim 9 wherein the branch direction indications and the branch prediction qualifier indications are accessible based at least in part on one or more of instruction instance identifiers and gshare addresses.

11. (Original) The branch prediction storage of claim 10 wherein instruction instance identifiers include physical addresses, virtual addresses, and program counters.

12. (Original) The branch prediction storage of claim 9 wherein the branch prediction storage also includes entries for one or more of branch history patterns and branch target instruction instance identifiers.

13. (Original) The branch prediction storage of claim 9 wherein the branch prediction qualifier indications include one or more bits that indicate one or more of confidence, strength, and validity of branch direction indications.

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14. (Original) The branch prediction storage of claim 9 wherein the branch direction indications include one or more bits that indicate whether a branch is taken or not taken.

15. (Previously Presented) A method of operating a processor that supports branch prediction, the method comprising:

accessing a branch prediction structure connected to a bus for carrying at least a portion of an instruction instance identifier that corresponds to a branch instruction instance;

determining from the branch prediction structure a branch direction indication that corresponds to said at least a portion of the instruction instance identifier; and

determining from the branch prediction structure a branch prediction qualifier indication that corresponds to said at least a portion of the instruction instance identifier,

wherein the branch prediction structure includes more entries for branch direction indications than entries for branch prediction qualifier indications;

said branch direction indication indicates a direction of said branch instruction instance with respect to branch prediction and the branch direction indication is associated with said at least a portion of the instruction instance identifier; and

an outcome of said branch instruction instance is predicted based at least in part on said branch direction indication and said branch prediction qualifier.

16. (Original) The method of claim 15 wherein determining the branch direction indication and the branch prediction

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qualifier indication is based at least in part on the instruction instance identifier and at least in part on the least significant bits of the instruction instance identifier, respectively.

17. (Original) The method of claim 16 wherein determining the branch direction indication comprises obtaining one or more values from one or more operations on the instruction instance identifier and selecting the branch direction indication that corresponds to the value.

18. (Previously Presented) The method of claim 17 wherein determining the branch direction indication comprises selecting the branch prediction qualifier indication with least significant bits of the obtained one or more values.

19. (Previously Presented) The method of claim 18 wherein at least some of the least significant bits of the obtained one or more values are unchanged from the instruction instance identifier.

20. (Original) The method of claim 15 further comprising determining one or more of a branch history pattern and a branch target instruction instance identifier that corresponds to the instruction instance identifier.

21. (Original) The method of claim 20 further comprising determining the branch direction indication with the instruction instance identifier and one or more of the branch history pattern and the instruction instance identifier.

22. (Original) The method of claim 15 wherein the instruction instance identifier includes one or more of physical addresses, virtual addresses, and program counters.

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23. (Original) The method of claim 15 further comprising performing branch prediction based at least in part on the determined branch direction indication and the determined branch prediction qualifier indication.

24. (Original) The method of claim 15 further comprising updating the branch prediction qualifier indication and the branch direction indication with respect to outcome of the instruction instance that corresponds to the instruction instance identifier.

25. (Previously Presented) A method of operating a processor that supports branch prediction, the method comprising:

determining if an instruction instance is a branch instruction and if the instruction instance is represented in a branch prediction structure;

if the instruction instance is a branch instruction and is represented in the branch prediction structure,

selecting in the branch prediction structure a branch direction indication that corresponds to an instruction instance identifier that corresponds with the instruction instance, and

selecting in the branch prediction structure a branch prediction qualifier indication that corresponds to the instruction instance identifier; and

performing branch prediction wherein an outcome of said branch prediction is based at least in part on the branch direction indication and the branch prediction qualifier indication,

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wherein the branch prediction qualifier indication is aliased to multiple branch direction indications; and

said branch direction indication indicates a direction of said branch instruction with respect to branch prediction.

26. (Previously Presented) The method of claim 25 wherein the branch direction indication is selected based at least in part on one or more of least significant bits of the instruction instance identifier and least significant bits of a gshare address.

27. (Original) The method of claim 25 wherein the instruction instance identifier includes one or more of physical addresses, virtual addresses, and program counters.

28. (Original) The method of claim 25 further comprising updating the branch direction indication and the branch prediction qualifier based at least in part on an outcome of the instruction instance.

29. (Original) The method of claim 25 wherein the branch prediction qualifier indication is one or more bits that indicate one or more of confidence, strength, and validity of branch direction indications.

Claims 30 to 44 (Cancelled)

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